What is claimed is:

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- 1. A method of fabricating a flash memory device comprising the steps of:
- forming a tunnel oxide layer on a semiconductor substrate, the material of the tunnel oxide layer having a conduction band energy level lower than that of SiO₂; forming a floating gate on the tunnel oxide layer; forming an intergate dielectric layer on the floating gate;
 - forming a control gate on the intergate dielectric layer; forming a gate electrode by patterning the tunnel oxide layer, the floating gate, the intergate dielectric layer, and the control gate; and
- forming a source/drain region by performing an ion implantation into the substrate using the gate electrode as a mask.
 - 2. The method as defined by claim 1, wherein the tunnel oxide layer is made of one selected from the group consisting of Y_2O_3 , Al_2O_3 , HfO_2 , and ZrO_2 with a conduction band energy level lower than that of SiO_2 .
 - 3. The method as defined by claim 1, wherein the step of forming the tunnel oxide layer comprises the steps of: forming a first tunnel oxide layer on the semiconductor substrate; and
 - forming a second tunnel oxide layer on the first tunnel oxide layer.
 - 4. The method as defined by claim 3, wherein the first tunnel oxide layer is made of one selected from the group consisting of Y_2O_3 , Al_2O_3 , HfO_2 , and ZrO_2 with a conduction band energy level lower than that of SiO_2 .
 - 5. The method as defined by claim 3, wherein the second tunnel oxide layer is made of one selected from the group consisting of Y_2O_3 , Al_2O_3 , and SiO_2 with a

- conduction band energy level equal or similar to that of SiO_2 .
- 6. The method as defined by claim 3, wherein the first tunnel oxide layer is deposited more thickly than the second tunnel oxide layer.

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